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2 What is claimed is:

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5 1. A method of fabrication of a bond pad structure, comprising the steps of:

6 a) providing a top wiring layer and a top dielectric layer over a
7 semiconductor structure;

8 b) forming a buffer dielectric layer over said top wiring layer and said top
9 dielectric layer;

10 c) forming a buffer opening in said buffer dielectric layer exposing at
11 least of portion of said top wiring layer;

12 d) forming a barrier layer over said buffer dielectric layer, and said top
13 wiring layer in said buffer opening;

14 e) forming a conductive buffer layer over said barrier layer;

15 f) planarizing said conductive buffer layer to form a buffer pad in said
16 buffer opening;

17 g) forming a passivation layer over said buffer pad and said buffer
18 dielectric layer;

19 h) forming a bond pad opening in said passivation layer over at least a
20 portion of said buffer pad;

1 i) forming a bond pad support layer over said buffer pad and passivation
2 layer;

3 j) forming a bond pad layer over said bond pad support layer;

4 k) patterning said bond pad layer and said bond pad support layer to form
5 a bond pad and bond pad support.

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7 2. The method of claim 1 wherein said top wiring layer is comprised of Cu alloy; said top
8 wiring layer is a damascene interconnect.

9 3. The method of claim 1 wherein said top dielectric layer is comprised of oxide made
10 from tetraethylorthosilicate (TEOS) reactants and has a thickness between 6750 and
11 8250 Å.

12 4. The method of claim 1 wherein said top dielectric layer is comprised black diamond TM
13 film.

14 5. The method of claim 1 wherein said top dielectric layer is comprised an oxide based
15 low k dielectric material with a K equal or less than 3.0.

16 6. The method of claim 1 wherein said buffer dielectric layer is comprised of TEOS oxide
17 and has a thickness between 6750 and 8250 Å.

1 7. The method of claim 1 wherein said barrier layer is comprised of Ta or a bilayer
2 comprised of a Cr layer and a Cr-Cu layer; said barrier layer has a thickness
3 between 360 and 440 Å.

4 8. The method of claim 1 wherein said conductive buffer layer is comprised of an
5 aluminum alloy with between a 99.45 and 99. 55 wt % aluminum and between
6 0.45 and 0.55 wt % copper; said conductive buffer layer has a thickness between
7 6750 and 8250 Å.

8 9. The method of claim 1 wherein the planarization of said conductive buffer layer
9 comprises a chemical-mechanical polish step.

10 10. The method of claim 1 wherein said passivation layer is comprised of a three layer
11 structure of (1) lower silicon nitride layer, (2) undoped silicate glass layer and
12 (3) upper silicon nitride layer; and has a thickness between 13500 and 16500 Å.

13 11. The method of claim 1 wherein said bond pad opening has an area between 2500 and
14 10000 sq. μ m.

15 12. The method of claim 1 wherein said buffer opening is larger than said bond pad
16 opening; said buffer opening extends beyond said bond pad opening on all sides.

17 13. The method of claim 1 wherein said bond pad support layer is comprised of a material
18 selected from the group consisting of Ti, TiW, W and Cr; and has thickness
19 between 2000 and 6000 Å

1 14. The method of claim 1 wherein said bond pad layer comprised of an Al-Cu alloy with
2 Al between 99.45 and 99. 55 wt % and Cu between 0.45 and 0.55 % ; said bond
3 pad layer has a thickness between 6000 and 15000 Å; and said buffer pad underlies
4 the entire bond pad.

5 15. The method of claim 1 wherein said buffer pad underlies the entire bond pad; said
6 buffer pad has a larger area than said bond pad by between 10 % and 30 % of the
7 area of the bonding pad.

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9 16. A method of fabrication of a bond pad structure; comprising the steps of:

10 a) providing a top wiring layer and a top dielectric layer over a
11 semiconductor structure;

12 (1) said top wiring layer comprised of Cu alloy; said top wiring layer is a
13 damascene interconnect;

14 (2) said top dielectric layer is comprised of TEOS oxide and has a
15 thickness between 6750 and 8250 Å;

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17 b) forming a buffer dielectric layer over said top wiring layer and said top
18 dielectric layer;

1 (1) said buffer dielectric layer is comprised of TEOS oxide and has a
2 thickness between 6750 and 8250 Å;
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4 c) a buffer opening in said buffer dielectric layer exposing at least of
5 portion of said top wiring layer;
6 d) forming a barrier layer over said buffer dielectric layer, and said top
7 wiring layer in said buffer opening;
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9 (1) said barrier layer is comprised of Ta or a bilayer comprised of a Cr layer
10 and a Cr-Cu layer; said barrier layer has a thickness between 360 and
11 440 Å;
12 e) forming a conductive buffer layer over said barrier layer;
13
14 (1) said conductive buffer layer is comprised of an Aluminum alloy with
15 between a 99.45 and 99. 55 wt % aluminum and between 0.45 and
16 0.55 wt % copper; said conductive buffer layer has a thickness
17 between 6570 and 8250 Å;
18 f) planarizing said conductive buffer layer to form a buffer pad in said
buffer opening;

1 (1) the planarization of said conductive buffer layer comprises a chemical-
2 mechanical polish step;

3 g) forming a passivation layer over said buffer pad and said buffer
4 dielectric layer; said passivation layer is comprised of a three layer structure of
5 (1) lower silicon nitride layer, (2) undoped silicate glass (USG) layer, and (3)
6 upper silicon nitride layer; and has a thickness between 13500 and 16500 Å;

7 h) forming a bond pad opening in said passivation layer over at least a
8 portion of said buffer pad

9 i) forming a support layer over said buffer pad and said buffer dielectric
10 layer;

11 (1) said bond pad support layer is comprised of a material selected from the
12 group consisting of Ti, TiW, and Cr; and has thickness between 2000
13 and 6000 Å;

14 j) forming a bond pad layer over said bond pad support layer;

15 (1) said bond pad layer comprised of an Al-Cu alloy and said bond pad
16 layer has a thickness between 6000 and 15000 Å;

17 k) patterning said bond pad layer and said bond pad support layer to form
18 a bond pad and bond pad support;

1 (1) said buffer pad underlies the entire bond pad; said buffer pad has a
2 larger area than said bond pad by between 10 % and 30 % of the area
3 of the bonding pad.

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5 17. A bond pad structure comprising:

6 a) a top wiring layer and a top dielectric layer over a semiconductor
7 structure:

8 b) a buffer dielectric layer over said top wiring layer and said top dielectric
9 layer:

10 c) a buffer opening in said buffer dielectric layer exposing at least of
11 portion of said top wiring layer:

12 d) a buffer pad and a barrier layer over said buffer dielectric layer and said
13 top wiring layer in said buffer opening;

14 e) forming a passivation layer over said conductive buffer pad and said
15 buffer dielectric layer;

16 f) a bond pad opening in said passivation layer over at least a portion of

18 g) a bond pad and bond pad support over said passivation layer over at
19 least a portion of said buffer pad, in at least said bond pad opening.

- 1 18. The bond pad structure of claim 17 wherein said top wiring layer is comprised of Cu
- 2 alloy; said top wiring layer is a damascene interconnect.
- 3 19. The bond pad structure of claim 17 wherein said top dielectric layer is comprised of
- 4 TEOS oxide and has a thickness between 6750 and 8250 Å.
- 5 20. The bond pad structure of claim 17 said top dielectric layer is comprised black
- 6 diamond TM film.
- 7 21. The bond pad structure of claim 17 said top dielectric layer is comprised an oxide
- 8 based low k dielectric material with a K equal or less than 3.0.
- 9 22. The bond pad structure of claim 17 wherein said barrier layer is comprised of Ta or a
- 10 bilayer comprised of a Cr layer and a Cr-Cu layer; said barrier layer has a thickness
- 11 between 360 and 440 Å.
- 12 23. The bond pad structure of claim 17 wherein said conductive buffer layer is comprised
- 13 of an Aluminum alloy with between a 99.45 and 99. 55 wt % Aluminum and
- 14 between 0.45 and 0.55 wt % copper; said conductive buffer layer has a thickness
- 15 between 6750 and 8250 Å.
- 16 24. The bond pad structure of claim 17 wherein said passivation layer is comprised of a
- 17 three layer structure of (1) lower silicon nitride layer, (2) undoped silicate glass
- 18 layer and (3) upper silicon nitride layer; and has a thickness between 13500 and
- 19 16500 Å.

1 25. The bond pad structure of claim 17 wherein said bond pad support layer is comprised
2 of a material selected from the group consisting of Ti or TiW, and Cr; and has
3 thickness between 2000 and 6000 Å.

4 26. The bond pad structure of claim 17 wherein said bond pad layer comprised of an Al-Cu
5 alloy and said bond pad layer has a thickness between 6000 and 15000 Å; and said
6 buffer pad underlies the entire bond pad.

7 27. The bond pad structure of claim 17 wherein said buffer pad underlies the entire bond
8 pad; said buffer pad has a larger area than said bond pad by between 10 % and 30
9 % of the area of the bonding pad.

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